What is claimed is:

1. A semiconductor memory device, comprising:

a write data controller for receiving predetermined bits of data inputted through data input/output pins to generate plural bits of data, and a read data controller for serially converting the plural bits of data to generate serially converted data through one of the data input/output pins during a test operation; and

the write data controller for receiving plural bits of data inputted through the input/output pins to generate the plural bits of data, and the read data controller for receiving the plural bits of data to generate the plural bits of data through the data input/ output pins during a regular operation,

wherein the number of the plural bits is N times the number of the predetermined bits, N being a natural number.

2. The device of claim 1, wherein the write data controller comprises transmission gates for transferring the data inputted through the data input/output pins in response to a test control signal.

3. The device of claim 1, wherein the read data controller comprises a parallel to serial converter for serially converting the plural bits of data to generate serially converted data in sequence in response to a test control signal during the test read operation.

4. The device of claim 1, wherein the predetermined bits are four bits and the plural bits are 16 bits.

5. The device of claim 1, wherein the semiconductor memory device is a double data rate (DDR) memory device.

6. The device of claim 3, wherein the test control signal is set by inputting a mode setting code corresponding to the test control signal to a mode setting register during a mode setting operation.

7. A semiconductor memory device, comprising:

a write data controller for receiving n bits of data inputted through data input/ output pins to generate n times k bits of data, and a read data controller for serially converting the n times k bits of data by to generate k bits of data to one of the data input/ output pins in sequence during a test operation; and

the write data controller for receiving n times k bits of data inputted through data input/ output pins to generate the n times k bits of data, and the read data controller for receiving the n times k bits of data to generate n times k bits of data through the data input/output pins during a regular operation,

wherein n and k are natural numbers.

8. The device of claim 7, wherein the write data controller comprises transmission gates for transferring the data inputted through the data input/output pins in response to a test control signal.

9. The device of claim 7, wherein the read data controller comprises a parallel to serial converter for serially converting the n times k bits of data to generate k bits of data in sequence in response to a test control signal during the test read operation.

10. The device of claim 7, wherein the n bits are four bits and the n times k bits are 16 bits.

11. The device of claim 7, wherein the semiconductor device is a double data rate (DDR) memory device

12. The device of claim 9, wherein the test control signal is set by inputting a mode setting code corresponding to the test control signal to a mode setting register during a mode setting operation.

13. A method of testing a semiconductor memory device, comprising:

extending n bits of data inputted through data input/output pins to generate n times k bits of data, writing the n times k bits of data to a memory cell array, reading the n times k bits of data stored in the memory cell array, and serially converting the n times k bits of data to generate k bits of data, and outputting the k bits of data through one of the data input/output pins during a test operation; and receiving n times k bits of buffered data inputted through data input/ output pins to generate n times k bits of data, writing the n times k bits of data to a memory cell array, reading the n times k bits of data stored in the memory cell array, and receiving the n times k bits of data to generate n times k bits of data, and outputting the n times k bits of data through data input/output pins during a regular operation,

wherein n and k are natural numbers.

14. The method of claim 13, serially converting the n times k bits of data comprises serially converting the n times k bits of data in sequence in response to a test control signal during the test read operation.

15. The method of claim 13, wherein the n bits are four bits and the n times k bits are 16 bits.

16. The method of claim 13, wherein the semiconductor device is a double data rate (DDR) memory device.

17. The method of claim 13 further comprising, inputting a mode setting code corresponding to the test control signal to a mode setting register during a mode setting operation.